Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (currently amended): A method comprising:

receiving a digital communication signal;

arranging said digital communication signal into an *rxn* matrix;

linear transforming the *rxn* matrix of at least one n-dimensional input vector in a ~~above the~~ real or complex or a finite field by:

storing in memory information about omitted rows, with respect to a selected row, in the matrix that are equivalent to one or more ~~duplicate of~~ other rows in the matrix, including the selected row ~~and rows in the matrix which includes information that is not duplicated in other rows~~;

omitting zero columns of said matrix and ~~the~~ corresponding scalar components of the input vector;

normalizing one or more ~~each~~ columns of said matrix by multiplying the one or more columns by one or more lead element inverses of the one or more columns~~, based on duplicate rows, and marking said duplicate rows as omitted rows~~;

generating a modified vector from groups in the normalized matrix;

generating a modified matrix; and

obtaining the output vector as indicative of said digital communication based at least in part on the omitted rows information.

2. (original): The method of Claim 1, further comprising splitting the transformation matrix into several sub-matrices

and obtaining the output vector by unifying the output vectors resulting from the products of each sub-matrix.

3. (original): The method of Claim 2, wherein the modified matrix encompasses a subset of rows of said transformation matrix.

4. (original): The method of Claim 3, further comprising splitting the input vector into several sub-vectors such that each sub-vector corresponds to a sub-matrix and wherein the output vector is obtained by adding the output vectors resulting from the products of each sub-matrix.

5. (previously presented): The method of Claim 1, further comprising splitting a modified matrix into several sub-matrices, wherein an output vector is obtained by adding the output vectors resulting from the products of each sub-matrix, by the respective sub-vector.

6. (original): The method of Claim 1, further comprising normalizing each column of said matrix by multiplying the column by the inverse of a lead element.

7. (original): The method of Claim 1, wherein the output vector is a product of the matrix and the input vector.

8. (original): The method of Claim 1, further comprising identifying groups of equal columns in the normalized matrix and attaching a unique location to each identified group.

9. (previously presented): An apparatus for performing a linear transformation, comprising:

first and second inputs which receive input data and predetermined data;

transformation circuitry which acts on the input data and predetermined data;

control and address generation circuitry, connected to a first memory, which generates corresponding addresses for accessing cells of said memory, and for controlling the selection between a data receiving mode, in which data is received via said first input, and a data processing mode, in which the arrival of incoming data via said first input is blocked; and

counter circuitry for controlling the timing of the operations of the apparatus;

wherein the control and address generation circuitry comprises:

a second memory which stores pre-programmed processing and control data;

a comparator circuitry which switches between the data receiving mode and the data processing mode;

a first set of multiplexers, each of which having at least one direct input for receiving transformation data, and another input, into which said transformation data is fed via a corresponding inverter, said first set being controlled to

transfer transformation data or, inverted transformation data, by a predetermined value provided by said transformation data;

a second set of multiplexers, each of which having at least one input connected to the output of a corresponding multiplexer selected from said first set of multiplexers, and another input, connected to said second memory, said second set being controlled by said comparator circuitry to provide a first address to the first memory by transferring the output of each multiplexer from said first set to the output of its corresponding multiplexer from said second set or, to provide at least a portion of the second address to the first memory by transferring data stored in said second memory; and

a multiplexer, operating in combination with said second set of multiplexers in said data processing mode, having an unconnected input and an input connected to said second memory and controlled by said comparator circuitry, thereby providing the remaining portion of said second address.

10. (original): The apparatus of claim 9, wherein the transformation circuitry multiplies each element of the input data by a corresponding element of the transformation data.

11. (original): The apparatus of claim 10, wherein the transformation circuitry comprises a memory which stores the result of the multiplication.

12. (original): The apparatus of claim 9, wherein the transformation circuitry comprises summation and accumulation circuitry.

13. (original): The apparatus of claim 9, further comprising a multiplexer circuitry which selects between the data receiving mode and the data processing mode.

14 - 15 (cancelled)

16. (new): A machine-implemented method comprising:

modifying an initial *rxn* transformation matrix to produce a modified matrix having reduced dimensions, said modifying comprising

identifying a group of equivalent rows if present, selecting a row from the equivalent rows group to retain, omitting one or more equivalent rows in the equivalent rows group, and storing in memory a ratio between each omitted row and the selected row,

omitting zero columns of said initial transformation matrix,

normalizing remaining columns of said initial transformation matrix by multiplying the remaining columns by inverses of their lead elements, respectively, to produce a normalized matrix, and

identifying a group of equal columns in the normalized matrix, selecting a column from the equal columns group to retain, and omitting one or more equal columns in the equal columns group;

receiving an n-dimensional input vector corresponding to a signal on a channel;

generating a modified vector from the n-dimensional input vector according to the modified matrix by omitting elements of

the input vector corresponding to the omitted zero columns, normalizing the input vector by multiplying elements of the input vector by the lead elements used in normalizing the remaining columns of the initial transformation matrix, and summing normalized input vector elements according to the identified equal columns group; and

obtaining an r-dimensional output vector by multiplying the modified vector by the modified matrix, said obtaining comprising

accumulating sums of elements of the modified vector according to the modified matrix, and

generating elements of the r-dimensional output vector that correspond to the one or more omitted rows using the stored one or more ratios in the memory.

17. (new): The method of Claim 16, wherein modifying the initial *rxn* transformation matrix further comprises splitting the transformation matrix into several sub-matrices and obtaining the r-dimensional output vector further comprises unifying multiple output vectors resulting from products of each sub-matrix.

18. (new): The method of claim 17, wherein the modified matrix encompasses a subset of rows of said transformation matrix.

19. (new): The method of claim 18, further comprising splitting the input vector into several sub-vectors such that each sub-vector corresponds to a sub-matrix and wherein the

output vector is obtained by adding the output vectors resulting from the products of each sub-matrix.

20. (new): The method of claim 16, further comprising splitting the modified matrix into several sub-matrices, wherein an output vector is obtained by adding output vectors resulting from products of each sub-matrix by respective corresponding sub-vectors.

21. (new): An apparatus for performing a linear transformation, comprising:

first and second inputs that receive input data and predetermined transformation data from means for reducing dimensions of and normalizing general real and complex matrices corresponding to linear transformations;

transformation and accumulation circuitry that acts on the input data and the predetermined transformation data to produce an output vector of a linear transformation corresponding to the predetermined transformation data, wherein the transformation and accumulation circuitry comprises an adder and a memory;

control and address generation circuitry, connected to the transformation and accumulation circuitry, wherein the control and address generation circuitry generates corresponding addresses for accessing cells of said memory, and for controlling selection between a data receiving mode, in which the input data is received via said first input and stored in the memory according to addresses corresponding to matrix columns, and a data processing mode, in which accumulating operations add or subtract data from one cell of the memory to another cell of the memory; and

counter circuitry for controlling timing of operations in the apparatus.

22. (new): The apparatus of claim 21, wherein the transformation and accumulation circuitry further comprise a first multiplier that multiplies each element of the input data by a corresponding element of the transformation data during the data receiving mode, and a second multiplier that multiplies data from the memory with a sign output of the control and address generation circuitry during the data processing mode.

23. (new): The apparatus of claim 22, wherein the memory comprises a dual port random access memory.

24. (new): The apparatus of claim 21, further comprising a multiplexer circuitry which selects between the data receiving mode and the data processing mode based on an output of the control and address generation circuitry.